Chapter 7
Gate Drive circuit Design

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This section explains the drive circuit design.

In order to maximize the performance of an IGBT, it is important to properly set the drive circuit constants.

1 IGBT drive conditions and main characteristics

IGBT drive conditions and main characteristics are shown below. An IGBT's main characteristics change according to the values of VGE and RG, so it is important to use settings appropriate for the intended use of the equipment in which it will be installed.

Table 7-1 IGBT drive conditions and main characteristics.

Main characteristics	$+V_{GE}$ rise	$–V_{GE}$ rise	R_G rise
$V_{CE(sat)}$	Fall	-	-
t_{on} E_{on}	Fall	-	Rise
t_{off} E_{off}	-	Fall	Rise
Turn-on surge voltage	Rise	-	Fall
Turn-off surge voltage	-	Rise	Fall
dv/dt malfunction	Rise	Fall	Fall
Current limit value	Rise	-	Fall
Short circuit withstand capability	Fall	-	Rise *1
Radiational EMI noise	Rise	-	Fall

*: Non latch-up circuit is built into N series IGBT. Short circuit withstand capability depends on current limiting circuit characteristic.

1.1 $+V_{GE}$ (On state)

A recommended the gate on state voltage value (+ V_{GE}) is +15V. Notes when + V_{GE} is designed are shown as follows.

(1) Set $+V_{GE}$ so that is remains under the maximum rated G-E voltage, V_{GES} =±20V.
(2) It is recommended that supply voltage fluctuations are kept to within ±10%.
(3) The on-state C-E saturation voltage $V_{GE(sat)}$ is inversely dependent on $+V_{GE}$, so the greater the $+V_{GE}$ the smaller the $V_{GE(sat)}$.
(4) Turn-on switching time and switching loss grow smaller as $+V_{GE}$ rises.
(5) At turn-on (at FWD reverse recovery), the higher the $+V_{GE}$ the greater the likelihood of surge voltages in opposing arms.
(6) Even while the IGBT is in the off-state, there may be malfunctions caused by the dv/dt of the FWD's reverse recovery and a pulse collector current may cause unnecessary heat generation. This phenomenon is called a dv/dt shoot through and becomes more likely to occur as $+V_{GE}$ rises.
(7) In U series IGBTs, the higher the $+V_{GE}$, the higher the current limit becomes.
(8) The greater the $+V_{GE}$ the smaller the short circuit withstand capability.

1.2 $-V_{GE}$ (Off state)

A recommended the gate reverse bias voltage value ($-V_{GE}$) is –5 to -15V. Notes when $-V_{GE}$ is designed are shown as follows.

(1) Set $-V_{GE}$ so that it remains under the maximum rated G-E voltage, V_{GES} =±20V .
(2) It is recommended that supply voltage fluctuations are kept to within ±10%.
(3) IGBT turn-off characteristics are heavily dependent on $-V_{GE}$, especially when the collector current is just beginning to switch off. Consequently, the greater the $-V_{GE}$ the shorter, the switching time and the switching loss become smaller.

(4) If the $-V_{GE}$ is too small, dv/dt shoot through currents may occur, so at least set it to a value greater than –5V. If the gate wiring is long, then it is especially important to pay attention to this.

1.3 R_G (Gate resistance)

Listed in the product specification sheets under the heading of switching time using standard gate resistance. . Notes when R_G is designed are shown as follows.

(1) The switching characteristics of both turn-on and turn-off are dependent on the value of R_G, and therefore the greater the R_G the longer the longer the switching time and the greater the switching loss. Also, as R_G increases, the surge voltage during switching becomes smaller.
(2) The greater the R_G the more unlikely a dv/dt shoot through current becomes.
(3) N and S series IGBT modules have a built in overcurrent limiting capability and this overcurrent limit as well as the short circuit withstand capability are dependent on the value of R_G The greater the R_G the greater the short circuit withstand capability becomes, but conversely the current limit will drop. Therefore, it is important to set the overcurrent trip level of the equipment the modules will be installed in, to a value below this limit. At the recommended R_G value (Tj = 25°C), the lowest current limit point will be twice the rated current value.

Select the most suitable gate drive conditions while paying attention to the above points of interdependence.

2 Drive current

Since an IGBT has a MOS gate structure, to charge and discharge this gate when switching, it is necessary to make gate current (drive current) flow. Fig. 7-1 shows the gate charge (dynamic input) characteristics. These gate charge dynamic input characteristics show the electric load necessary to drive the IGBT and are used to calculate values like average drive voltage and the driving electric power. Fig. 7-2 shows the circuit schematic as well as the voltage and current waveforms. In principle, a drive circuit has a forward bias power supply alternately switching back and forth using switch S_1 and S_2. During this switching, the current used to charge and discharge the gate, is the driven current. In Fig. 7-2 the area showing the current waveform (the hatched area) is equivalent to the gate charge from Fig. 7-1.

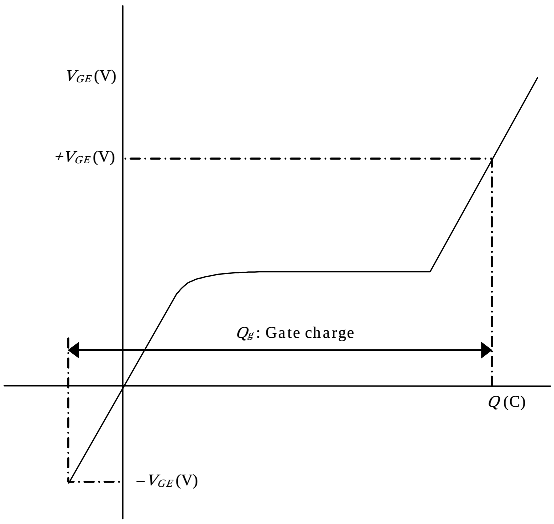

Fig. 7-1 Gate charge characteristics (Dynamic input characteristics).

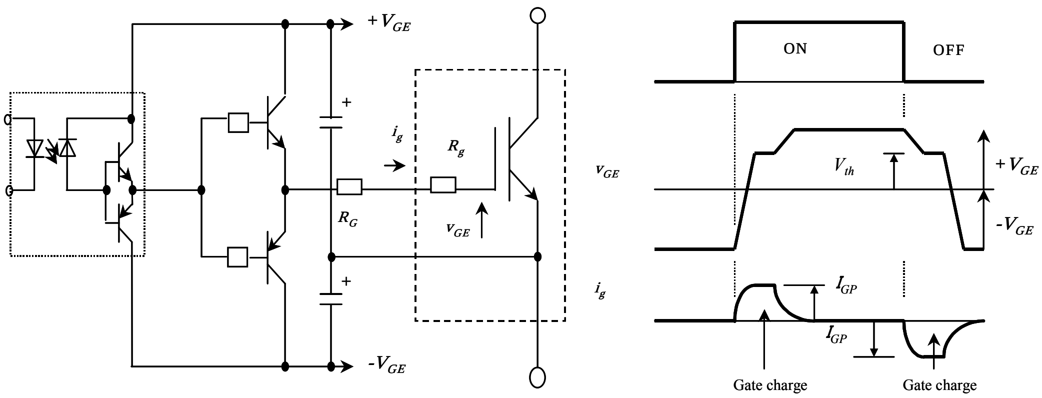

Fig. 7-2 Drive circuit schematic as well as voltage and current waveforms.

The drive current peak value I_{GP} can be approximately calculated as follows:

$$I_{GP} = \frac{+V_{GE} + \left|-V_{GE}\right|}{R_G + R_g}$$

$+V_{GE}$: Forward bias supply voltage
$-V_{GE}$: Reverse bias supply voltage
R_G : Drive circuit gate resistance
R_g : Module's internal resistance

Table 7-2 is shown in U series IGBT module internal gate resistance.

Table 7-2 U series IGBT module internal gate resistance.

Module withstand voltage (V)	Rated current (A)	Internal gate resistance (Ω)
600V	~ 200A	0 (None)
	300A, 400A	2.5
	600A	1.7
1200V	~ 50A	0 (None)
	75A ~ 150A	5
	150A ~ 300A (2 in 1)	2.5 (except 34 mm)
	300A (2 in 1)	2.5 (62 mm package) 1.7 (80 mm package)
	225A ~ 300A (6 in 1) A	1.7
	450A	1, 7
	600A, 800A	0.63

The slope of the gate charge characteristics (Refer to each modules technical specification sheets), rising from 0V is essentially the same as that of the input capacitance (Cies), and the reverse bias area can also be considered an extension of this. Therefore, the average value of the drive current IG, using the gate charge characteristics (Fig. 7-1), can be calculated as follows:

$$+I_G = -I_G = fc \times \left(Q_g + C_{ies} \times \left|-V_{GE}\right|\right)$$

fc : Carrier frequency
Q_g : Gate charge from 0V to $+V_{GE}$
C_{ies} : IGBT input capacitance

Consequently, it is important to set the output stage of the drive circuit in order to conduct this approximate current flow (IGB, as well as ±IG).
Furthermore, if the power dissipation loss of the drive circuit is completely consumed by the gate resistance, then the drive power (Pd) necessary to drive the IGBT is shown in the following formula:

$$Pd(on) = fc \bullet \left(\frac{1}{2} Q_g \left|+V_{GE}\right| + \frac{1}{2} C_{ies} \left|-V_{GE}\right|^2\right)$$

$$Pd(off) = Pd(on)$$

$$\begin{aligned} Pd &= Pd(off) + Pd(on) \\ &= fc \bullet \left(Q_g \left|+V_{GE}\right| + C_{ies} \left|-V_{GE}\right|^2\right) \end{aligned}$$

Accordingly, a gate resistance is necessary that can charge this approximate capacity.
Be sure to design the drive circuit so that the above mentioned drive current and drive power can be properly supplied.

3 Setting dead-time

For inverter circuits and the like, it is necessary to set an on-off timing "delay" (dead time) in order to prevent short circuits. During the dead time, both the upper and lower arms are in the "off" state. Basically, the dead time (see Fig. 7-3) needs to be set longer than the IGBT switching time (toff max.). Accordingly, if RG is increased, switching time also becomes longer, so it would be necessary to lengthen dead time as well. Also, it is necessary to consider other drive conditions as well as the modules distribution and temperature characteristics, etc. (at high temperatures, toff becomes longer). It is important to be careful with dead times that are too short, because in the event of a short circuit in the upper or lower arms, the heat generated by the short circuit current may destroy the module.

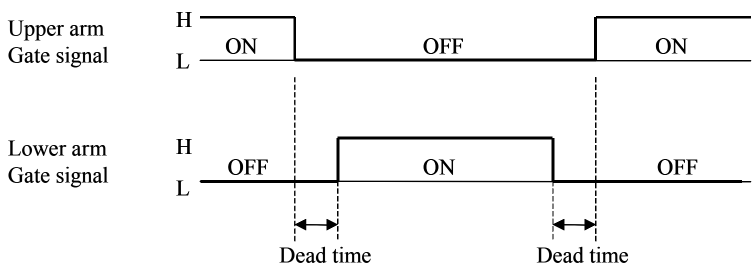

Fig. 7-3 Dead time timing chart.

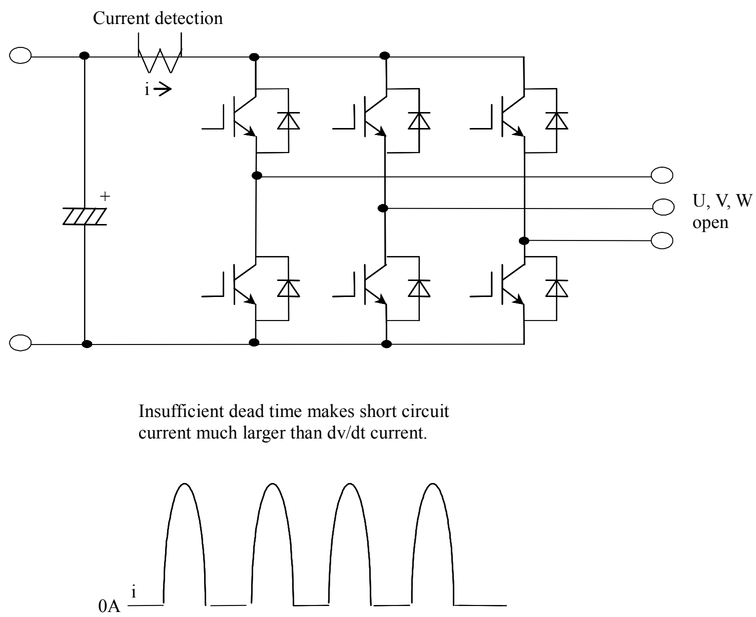

Fig. 7-4 Current detection methods for short circuit cased by insufficient dead time.

One method of judging whether or not the dead time setting is sufficient or not, is to check the current of a no-load DC supply line.
In the case of a 3-phase inverter (as shown in Fig. 7-4), set the inverter's outputs to open, then apply a normal input signal, and finally measures the DC line current. A very small pulse current (dv/dt current leaving out the module's Miller Capacitance: about 5% of the normal rated current) will be observed, even if the dead time is long enough.

However, if the date time is insufficient, then there will be a short circuit current flow much larger than this. In this case, keep increasing the dead time until the short circuit current disappears. Also, for the same reasons stated above, we recommend testing at high temperatures.

4 Concrete examples of drive circuits

For inverter circuits and the like, it is necessary to electrically isolate the IGBT from the control circuit. An example of a drive circuit using this principle, is shown below.
Fig. 7-5 shows an example of a drive circuit using a high speed opto-coupler. By using the opto-coupler, the input signal and the module are isolated from each other. Also, since the opto-coupler does not limit the output pulse width, it is suitable for changing pulse widths or PWM controllers, to wide ranges. It is currently the most widely used.
Furthermore, this way the turn-on and turn-off characteristics determined by gate resistance can be set separately, so it commonly used to ensure the best settings. Fuji Electric is switching using opto-couplers to implement their Hybrid-ICs. (See Table below.) Hybrid-ICs can drive with a single power supply, and also have a built in short circuit detection function as well as a soft cutoff circuit enabling them to provide the IGBT reliable protection in the event of a short circuit. For more complete details, refer to Hybrid-IC Application Manual. Aside from the above, there is also a signal isolation method using a pulse transformer. With this method the signal as well as the gate drive power can both be supplied simultaneously from the signal side, thereby allowing circuit simplification. However, this method has the limitations of an on/(off+on) time ratio of max. 50%, and reverse bias cannot be set, so its usefulness as a control method and switching frequency regulator is limited.

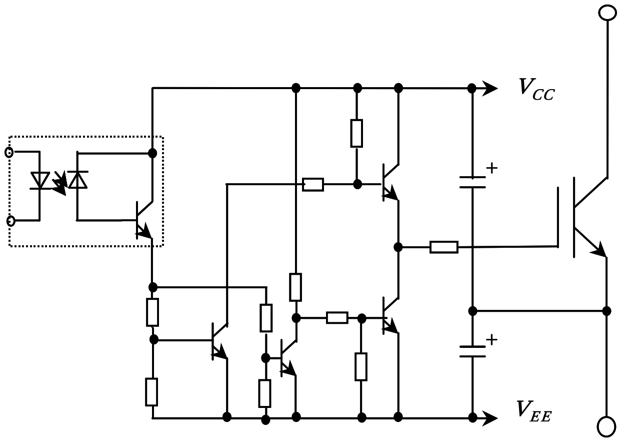

Fig. 7-5 Example of drive circuit using high speed opto-coupler.

Table 7-3 Hybrid ICs for driving IGBTs.

IGBT type / Suitable hybrid IC	600Vclass Up to 150A 1200Vclass Up to 75A	600Vclass 200A to 400A 1200Vclass 100A to 300A
Medium speed type	EXB850	EXB851
High speed type	EXB840	EXB841

Medium speed type: Drive circuit signal transmission delay 4μs max.
High speed type: Drive circuit signal transmission delay 1.5μs max.

5 Drive circuit setting and actual implementation

5.1 Opto-coupler noise ruggedness

As IGBTs are high speed switching elements, it is necessary to select a opto-coupler for drive circuit that has a high noise ruggedness (e.g. HCPL4504). Also, to prevent malfunctions, make sure that the wiring from different sides doesn't cross. Furthermore, in order to make full use of the IGBT's a high speed switching capabilities, we recommend using a opto-coupler with a short signal transmission delay.

5.2 Wiring between drive circuit and IGBT

If the wiring between the drive circuit and the IGBT is long, the IGBT may malfunction due to gate signal oscillation or induced noise. A countermeasure for this is shown below in Fig. 7-6.

(1) Make the drive circuit wiring as short as possible and finely twist the gate and emitter wiring. (Twist wiring)
(2) Increase RG. However, pay attention to switching time and switching loss.
(3) Separate the gate wiring and IGBT control circuit wiring as much as possible, and set the layout so that they cross each other (in order to avoid mutual induction).
(4) Do not bundle together the gate wiring or other phases.

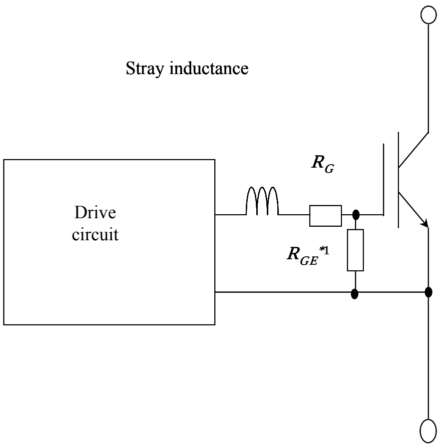

Fig. 7-6 Gate signal oscillation countermeasure

*1 R_{GE}
If the gate circuit is bad or if the gate circuit is not operating (gate in open state)*2 and a voltage is applied to the power circuit, the IGBT may be destroyed. In order to prevent this destruction, we recommend placing a 10kΩ resistance R_{GE} between the gate and emitter.
*2 Switch-on
When powering up, first switch on the gate circuit power supply and then when it is fully operational, switch on the main circuit power supply.

5.3 Gate overvoltage protection

It is necessary that IGBT modules, like other MOS based elements, are sufficiently protected against static electricity. Also, since the G-E absolute maximum rated voltage is ±20V, if there is a possibility that a voltage greater than this may be applied, then as a protective measure it is necessary to connect a zenner diode between the gate and emitter as shown in Fig. 7-7.

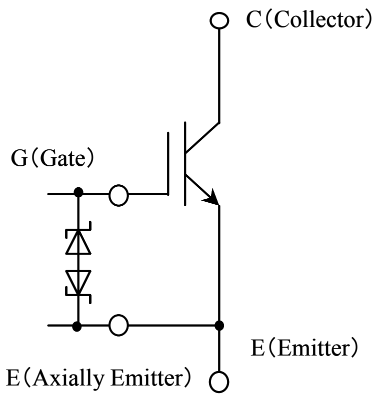

Fig. 7-7 G-E overvoltage protection circuit example.

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